

WHAT IS CLAIMED IS:

1. A method of forming a trench in a semiconductor device, comprising:

forming a sacrificial layer on a silicon wafer and selectively etching the sacrificial layer to form a LOCOS opening having a predetermined width;

5 performing thermal oxidation on a portion of the silicon wafer exposed through the LOCOS opening to form a LOCOS oxide layer;

etching the LOCOS oxide layer and the silicon wafer to a desired depth to form a trench, the etching being performed such that the LOCOS oxide layer is left remaining on the silicon wafer at an area corresponding to edges of the trench; and

10 forming an insulation layer such that the trench is filled with a material of the insulation layer.

2. The method of claim 1, wherein during formation of the LOCOS opening, one of a predetermined width of the sacrificial layer located at edges of a region where a trench is to be formed is etched, and the sacrificial layer is etched to a width greater by
15 a predetermined amount than a region to be occupied by a trench.

3. The method of claim 2, wherein in etching a predetermined width of the sacrificial layer located at edges of a region where a trench is to be formed, the sacrificial layer is etched to a width of 50-500 Å.

4. The method of claim 2, wherein in etching the sacrificial layer to a width greater by a predetermined amount than a region to be occupied by a trench, the sacrificial layer is etched having a width that is at most 400 Å greater than the trench.

5. The method of claim 1, wherein during formation of the trench, a photoresist layer is deposited on the LOCOS oxide layer and the sacrificial layer, then the photoresist layer is exposed and developed to form a photoresist layer pattern that exposes an area of the LOCOS oxide layer where a trench is to be formed, after which the photoresist layer pattern is used as a mask to etch the exposed area of the LOCOS oxide layer and the silicon wafer to a desired depth.

6. The method of claim 5, wherein the photoresist layer pattern is formed so that at most 200 Å of a width of the LOCOS oxide layer positioned at edges of the trench is covered such that at most 400 Å of an entire cross-sectional width is covered, and the remainder of the LOCOS layer is exposed.

7. The method of claim 1, further comprising forming a liner oxide layer prior to forming the insulation layer, the liner oxide layer covering inner walls of the trench and the remaining region of the LOCOS oxide layer.

8. The method of claim 7, wherein the liner oxide layer is formed to a thickness of 100-500 Å.

9. The method of claim 1, further comprising removing the remaining region of the LOCOS oxide layer and forming a liner oxide layer prior to forming the insulation layer.

10. The method of claim 9, wherein the liner oxide layer is formed to a thickness of 100-500 Å.

11. The method of claim 1, further comprising performing chemical-mechanical polishing on the insulation layer following the formation of the same until the sacrificial layer is exposed.

12. The method of claim 1, further comprising forming a pad oxide layer on the silicon wafer prior to forming the sacrificial layer, and forming the sacrificial layer on the pad oxide layer.

13. The method of claim 1, wherein the sacrificial layer is made of a material that is polished more slowly than the insulation layer that fills the trench.

14. The method of claim 1, wherein a nitride layer is used as the sacrificial layer.

15. The method of claim 14, wherein the nitride layer is formed to a thickness of 1500-3000 Å.

16. A trench in a semiconductor device used as a device isolation region formed in a silicon wafer, in which upper corner areas of the silicon wafer adjacent to the trench are rounded, and a LOCOS oxide layer is formed on the corner areas.

17. The trench of claim 16, wherein a liner oxide layer is formed on inner walls of the trench and on the LOCOS oxide layer.

18. The trench of claim 17, wherein the liner oxide layer is formed to a thickness of 100-500 Å.

5 19. The trench of claim 16, wherein the LOCOS oxide layer is formed to a thickness of at most 200 Å.

20. The trench of claim 19, wherein a liner oxide layer is formed along inner walls of the trench and on the LOCOS oxide layer, to a thickness of 100-500 Å.